FIG. 1

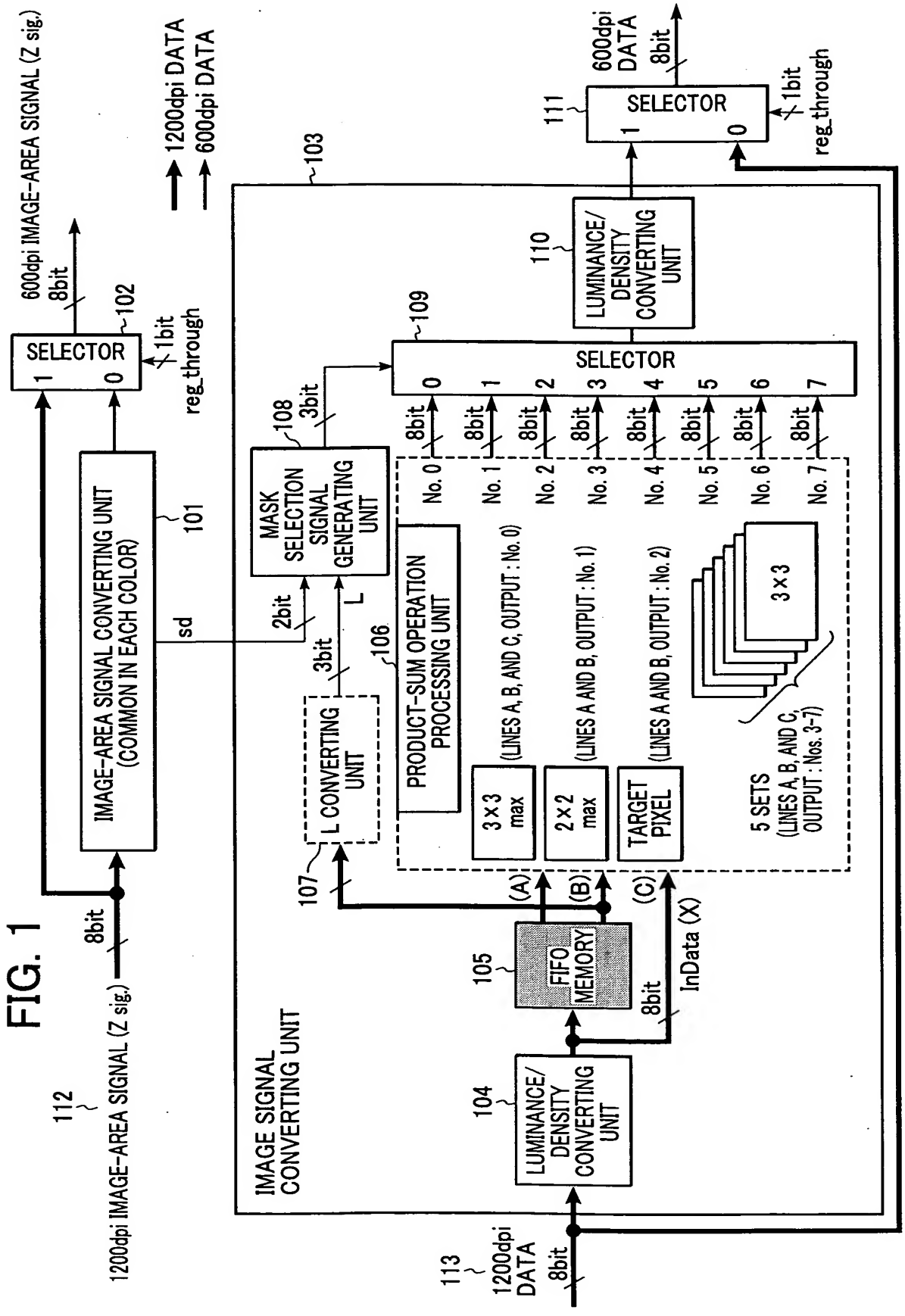

1200dpi IMAGE-AREA SIGNAL (Z sig.)
112
8bit
IMAGE-AREA SIGNAL CONVERTING UNIT (COMMON IN EACH COLOR)
101
sd
2bit
3bit
L
600dpi IMAGE-AREA SIGNAL (Z sig.)
8bit
SELECTOR
1
0
102
1bit
reg_through
1200dpi DATA
600dpi DATA
103
IMAGE SIGNAL CONVERTING UNIT
MASK SELECTION SIGNAL GENERATING UNIT
108
3bit
L CONVERTING UNIT
107
106
PRODUCT-SUM OPERATION PROCESSING UNIT
3×3 max
2×2 max
TARGET PIXEL
(LINES A, B, AND C, OUTPUT : No. 0)
(LINES A AND B, OUTPUT : No. 1)
(LINES A AND B, OUTPUT : No. 2)
3×3
5 SETS
(LINES A, B, AND C, OUTPUT : Nos. 3-7)
No. 0
No. 1
No. 2
No. 3
No. 4
No. 5
No. 6
No. 7
8bit
SELECTOR
109
0
1
2
3
4
5
6
7
LUMINANCE/ DENSITY CONVERTING UNIT
110
111
SELECTOR
1
0
600dpi DATA
8bit
1bit
reg_through
(A)
(B)
(C)
105
FIFO MEMORY
8bit
InData (X)
104
LUMINANCE/ DENSITY CONVERTING UNIT
113
1200dpi DATA
8bit

FIG. 2

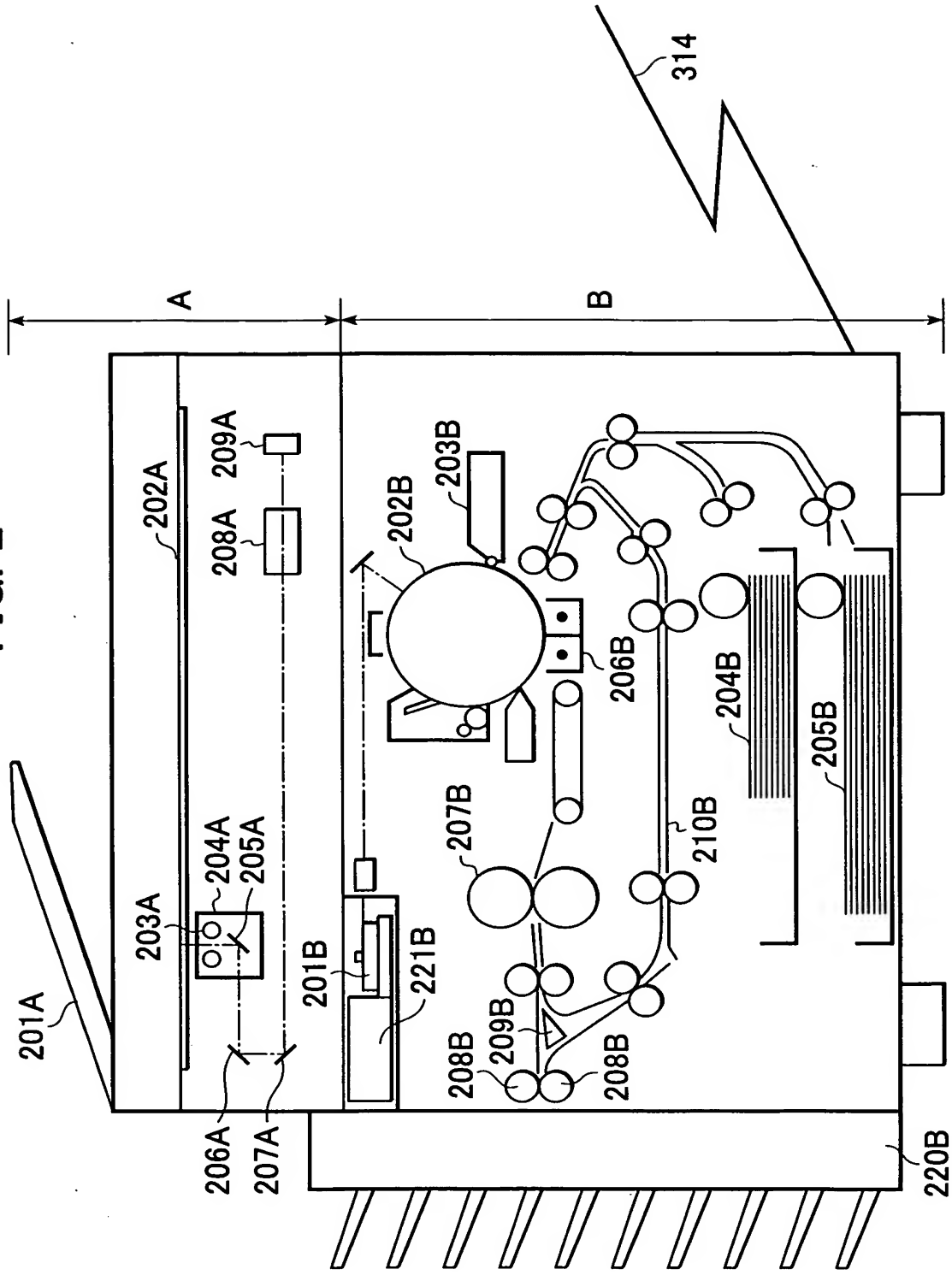

A
B
314
202A
209A
208A
203B
202B
206B
204B
205B
207B
210B
203A
204A
205A
201B
221B
201A
209B
208B
208B
206A
207A
220B

FIG. 3

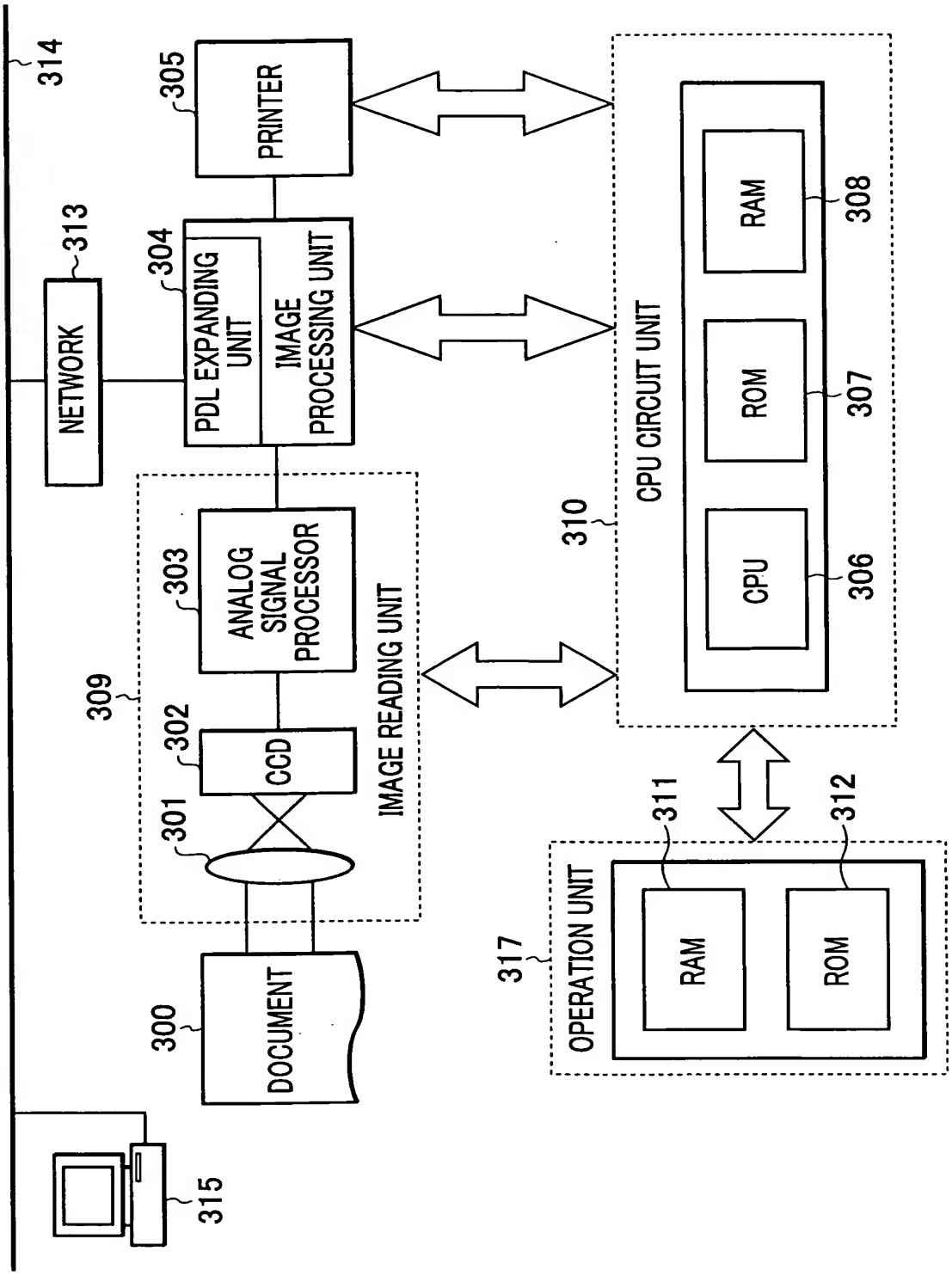

314
305
PRINTER
313
NETWORK
304
PDL EXPANDING UNIT
IMAGE PROCESSING UNIT
303
ANALOG SIGNAL PROCESSOR
309
302
CCD
301
IMAGE READING UNIT
300
DOCUMENT
315
310
CPU CIRCUIT UNIT
RAM
308
ROM
307
CPU
306
317
OPERATION UNIT
311
RAM
312
ROM

FIG. 4

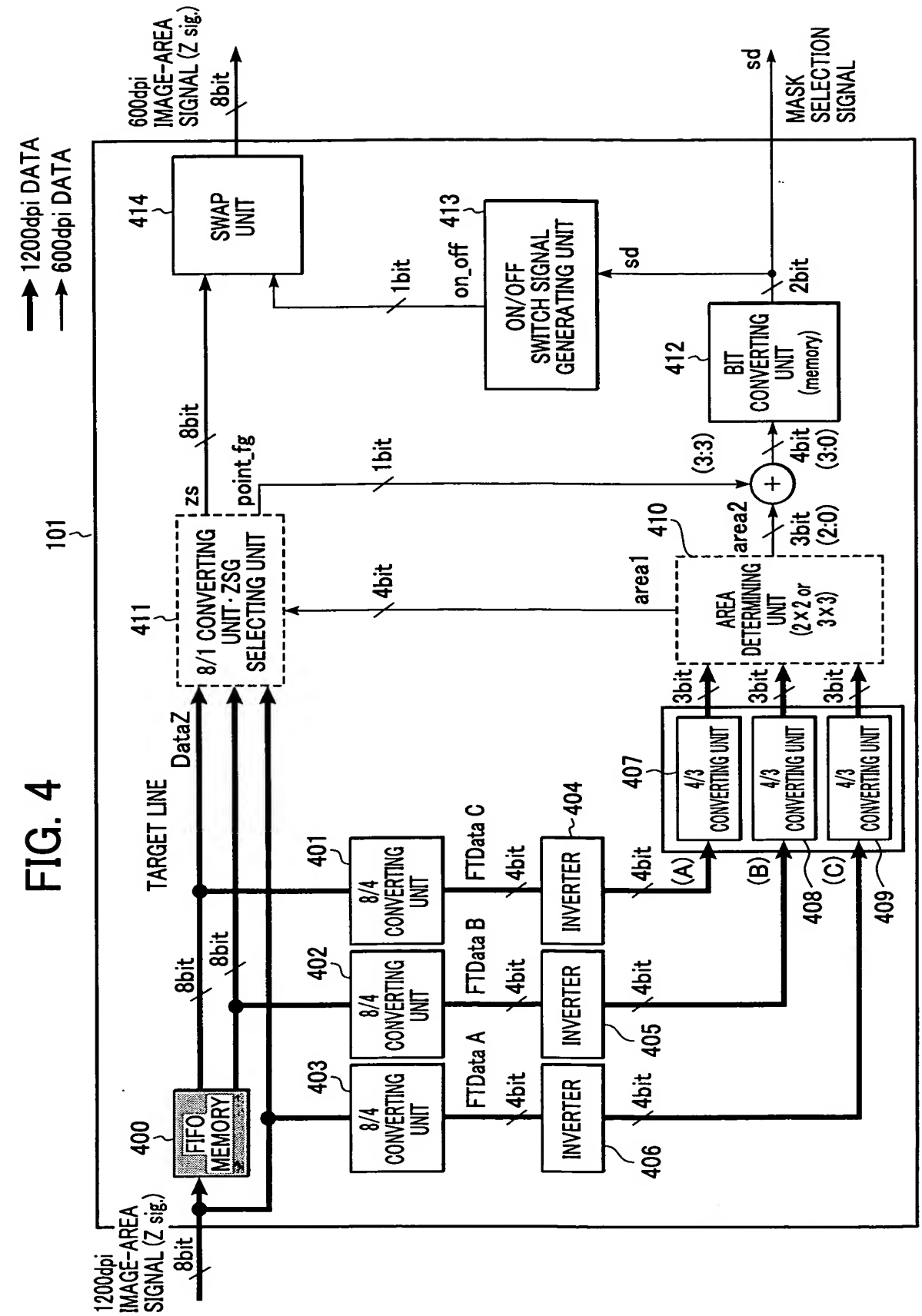

1200dpi DATA
600dpi DATA
101
1200dpi IMAGE-AREA SIGNAL (Z sig.)
8bit
400
FIFO MEMORY
TARGET LINE
DataZ
8bit
8bit
403
8/4 CONVERTING UNIT
402
8/4 CONVERTING UNIT
401
8/4 CONVERTING UNIT
FTData A
FTData B
FTData C
4bit
4bit
4bit
INVERTER
INVERTER
INVERTER
404
405
406
4bit
4bit
4bit
407
4/3 CONVERTING UNIT
4/3 CONVERTING UNIT
4/3 CONVERTING UNIT
3bit
3bit
3bit
(A)
(B)
(C)
408
409
411
8/1 CONVERTING UNIT·ZSG SELECTING UNIT
zs
8bit
point_fg
1bit
4bit
area1
410
AREA DETERMINING UNIT (2×2 or 3×3)
area2
3bit (2:0)
(3:3)
4bit (3:0)
412
BIT CONVERTING UNIT (memory)
2bit
sd
MASK SELECTION SIGNAL
413
ON/OFF SWITCH SIGNAL GENERATING UNIT
on_off
1bit
sd
414
SWAP UNIT
600dpi IMAGE-AREA SIGNAL (Z sig.)
8bit

FIG. 5

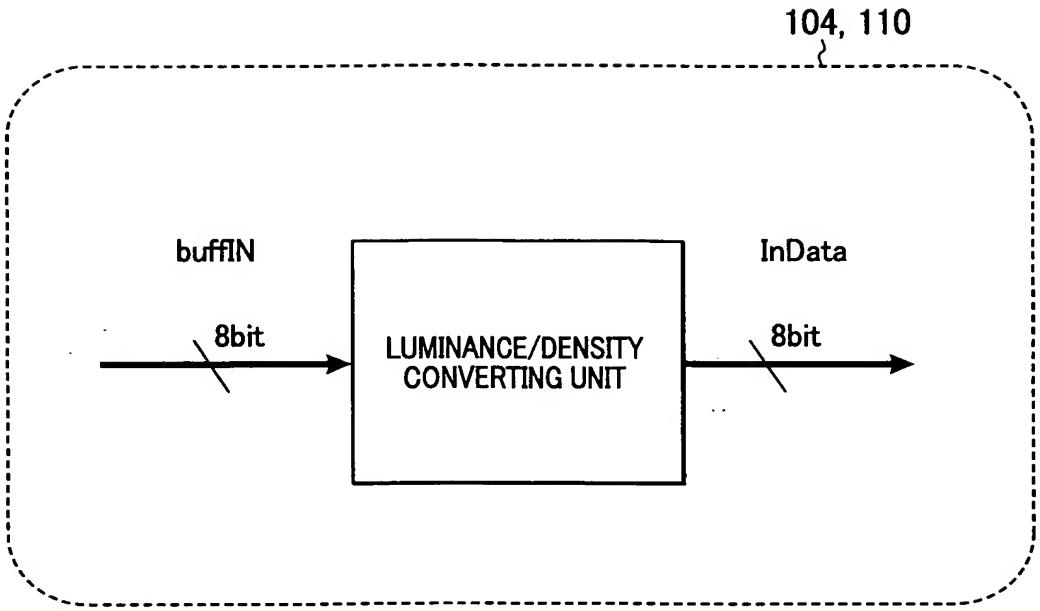

104, 110
buffIN
8bit
LUMINANCE/DENSITY CONVERTING UNIT
InData
8bit

FIG. 6A

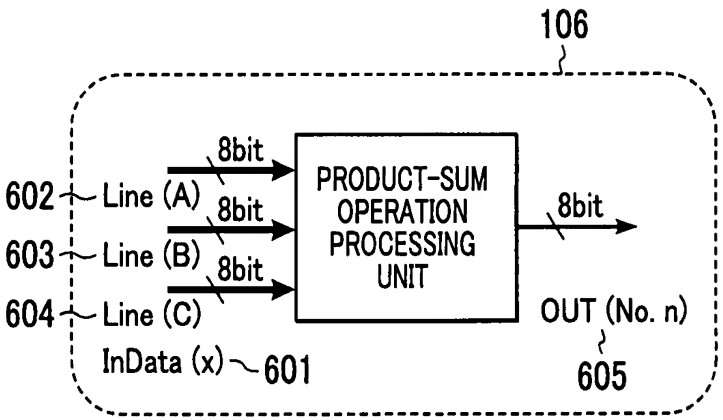


FIG. 6B

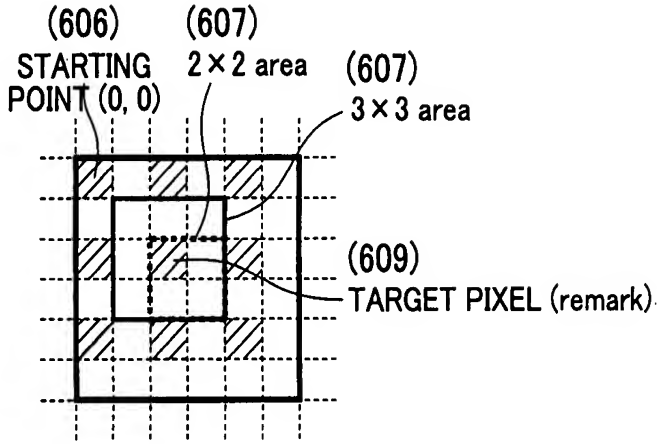


FIG. 6C

$$OUT = (a*x(i-1,j-1) + b*x(i,j-1) + c*x(i+1,j-1) + d*x(i-1,j) + e*x(i,j) + f*x(i+1,j) + g*x(i-1,j+1) + h(i,j+1) + i*x(i+1,j+1)) >> 6$$

if (OUT>255) OUT = 255 ;

x : IMAGE DATA (8 BITS)
a-i : MASK REGISTER 6 BITS

each team (under line) : 14bits
total : 18bits
last (out) : 8bits

610

a	b	c
d	e	f
g	h	i

MASK REGISTER (611)

$X_{(i-1,j-1)}$	$X_{(i,j-1)}$	$X_{(i+1,j-1)}$
$X_{(i-1,j)}$	$X_{(i,j)}$	$X_{(i+1,j)}$
$X_{(i-1,j+1)}$	$X_{(i,j+1)}$	$X_{(i+1,j+1)}$

IMAGE DATA (612)

FIG. 7

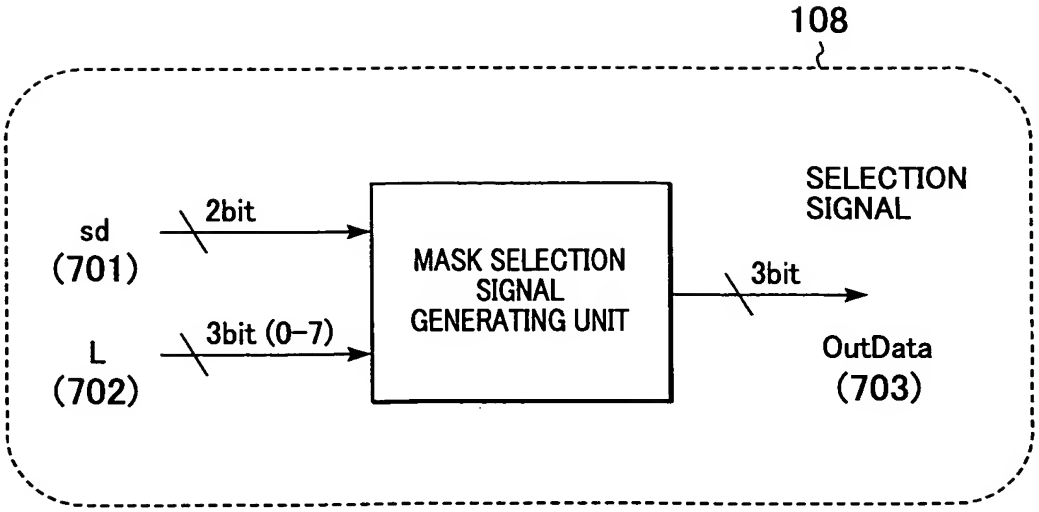

108
sd
(701)
2bit
L
(702)
3bit (0–7)
MASK SELECTION SIGNAL GENERATING UNIT
SELECTION SIGNAL
3bit
OutData
(703)

FIG. 8

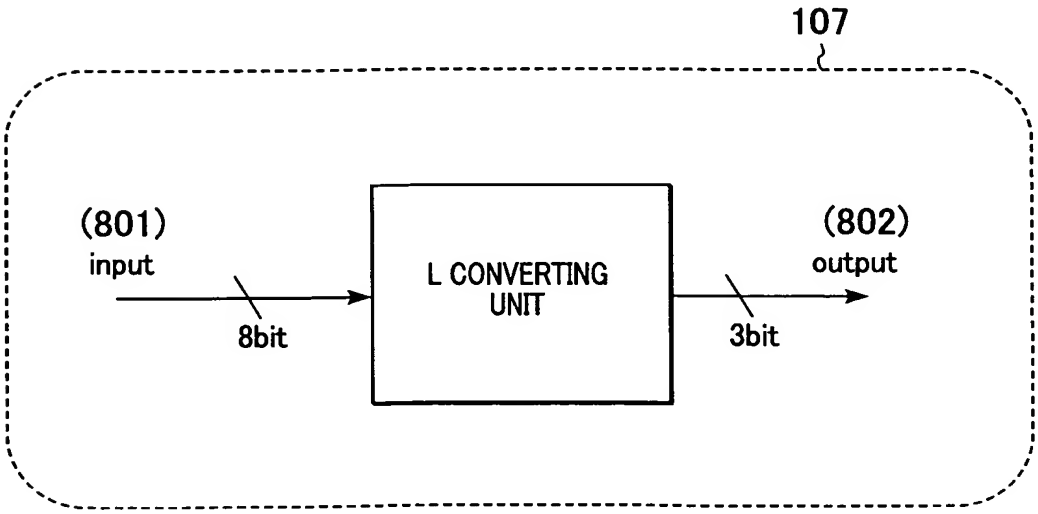

107
(801)
input
8bit
L CONVERTING UNIT
(802)
output
3bit

FIG. 9A

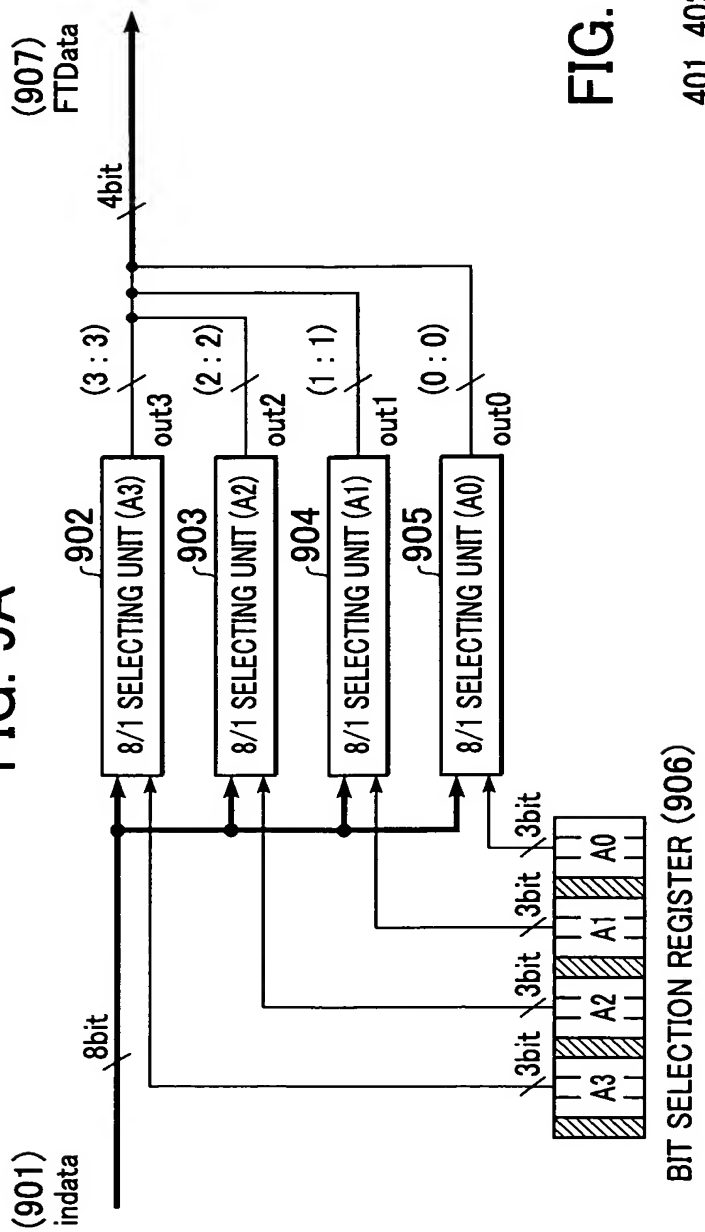

(907)
FTData
4bit
(3 : 3)
(2 : 2)
(1 : 1)
(0 : 0)
out3
out2
out1
out0
902
903
904
905
8/1 SELECTING UNIT (A3)
8/1 SELECTING UNIT (A2)
8/1 SELECTING UNIT (A1)
8/1 SELECTING UNIT (A0)
8bit
(901)
indata
3bit
3bit
3bit
3bit
A3
A2
A1
A0
BIT SELECTION REGISTER (906)

FIG. 9B

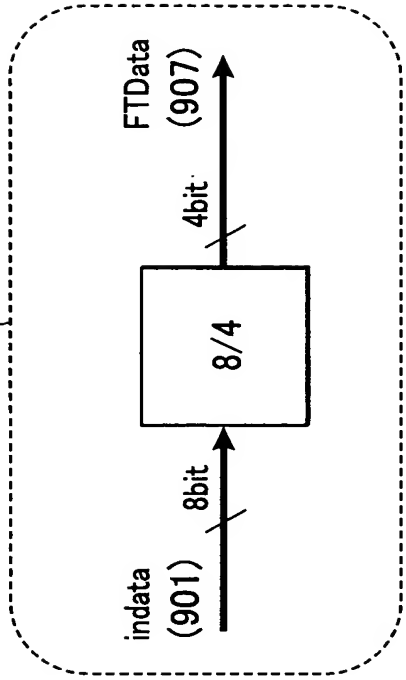

401, 402, 403
FTData
(907)
4bit
8/4
8bit
indata
(901)

FIG. 10A

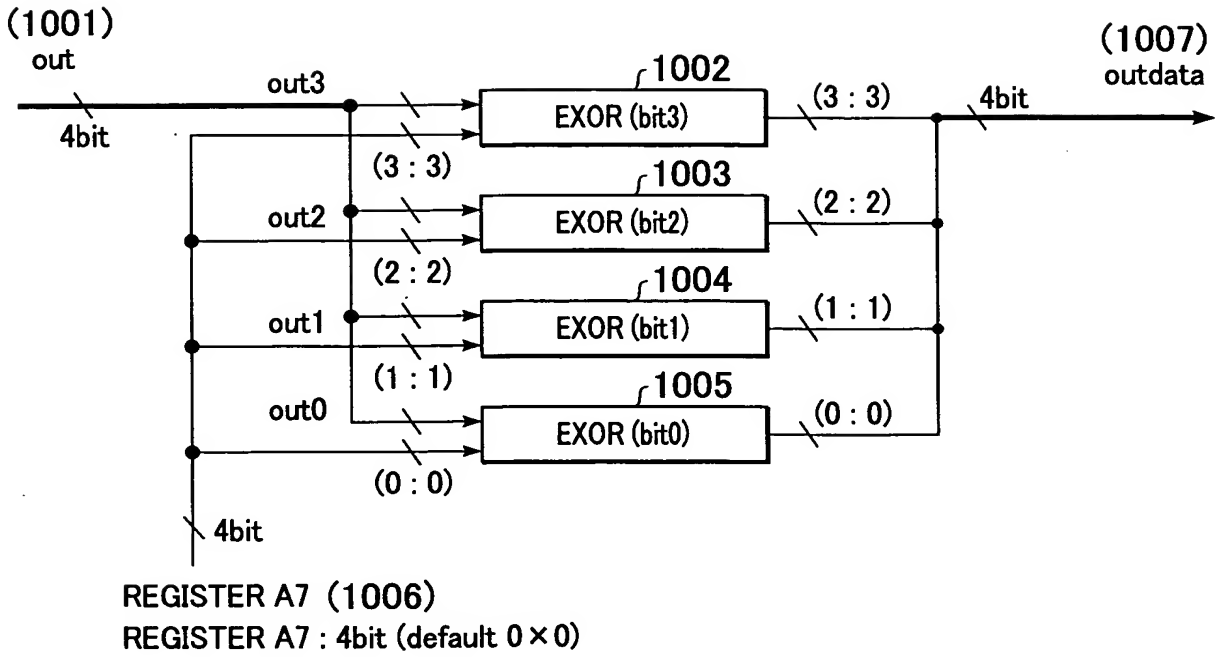


FIG. 10B

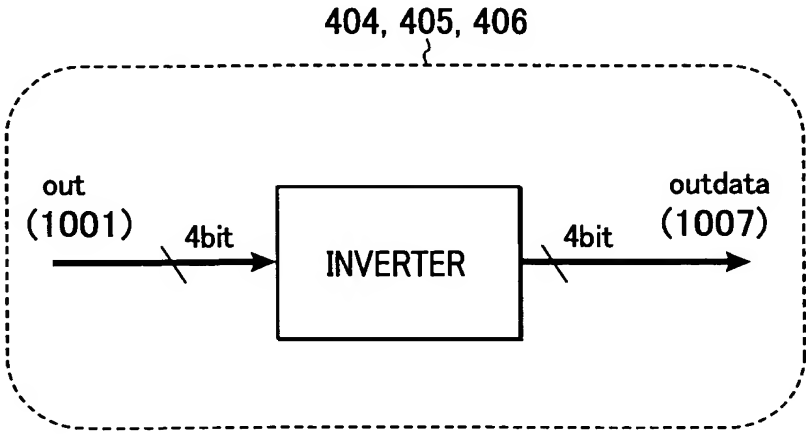
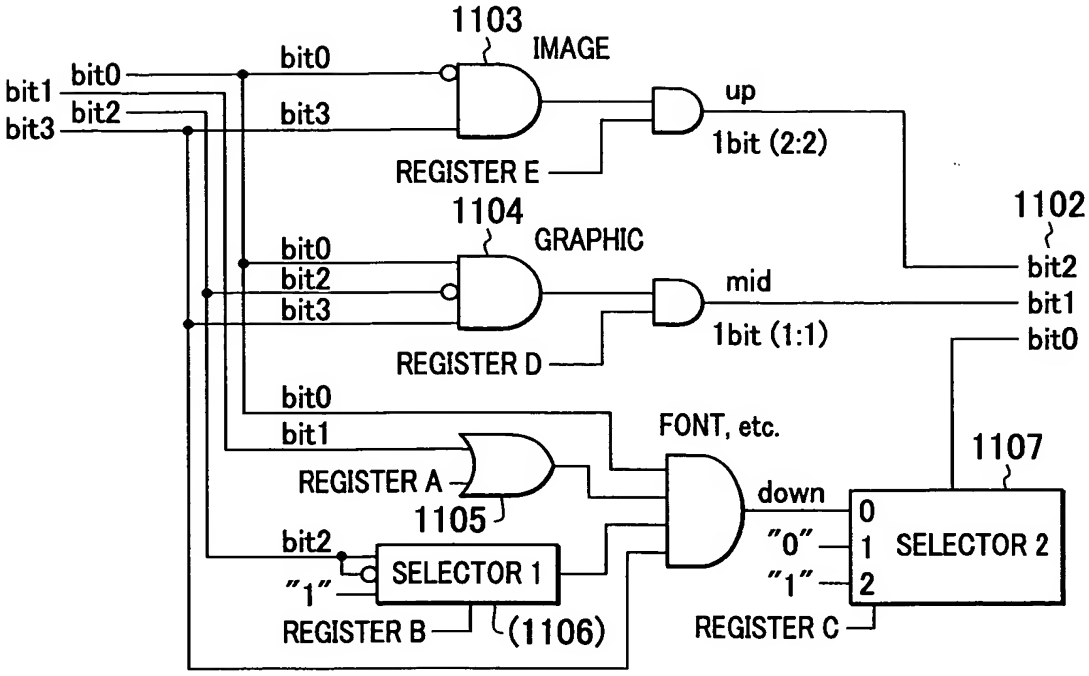


FIG. 11A



REGISTER A : 1 BIT (DEFAULT 0×1)
REGISTER B : 2 BITS (DEFAULT 0×0)
REGISTER C : 2 BITS (DEFAULT 0×0)
REGISTER D : 1 BIT (DEFAULT 0×1)
REGISTER E : 1 BIT (DEFAULT 0×1)

FIG. 11B

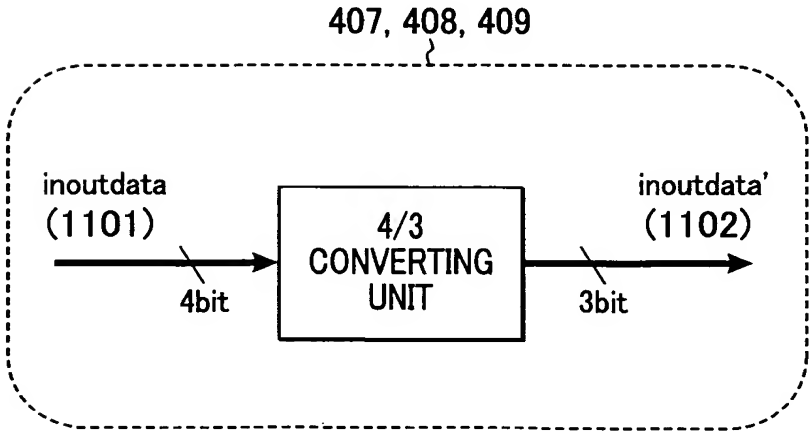


FIG. 12A

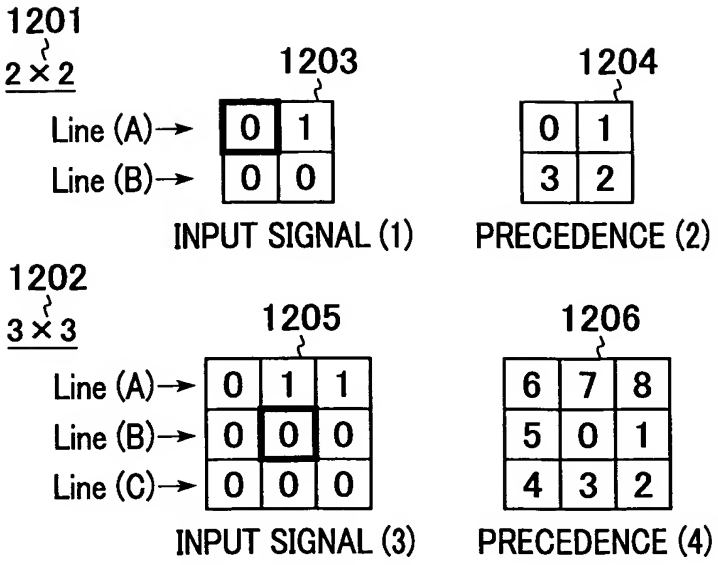


FIG. 12B

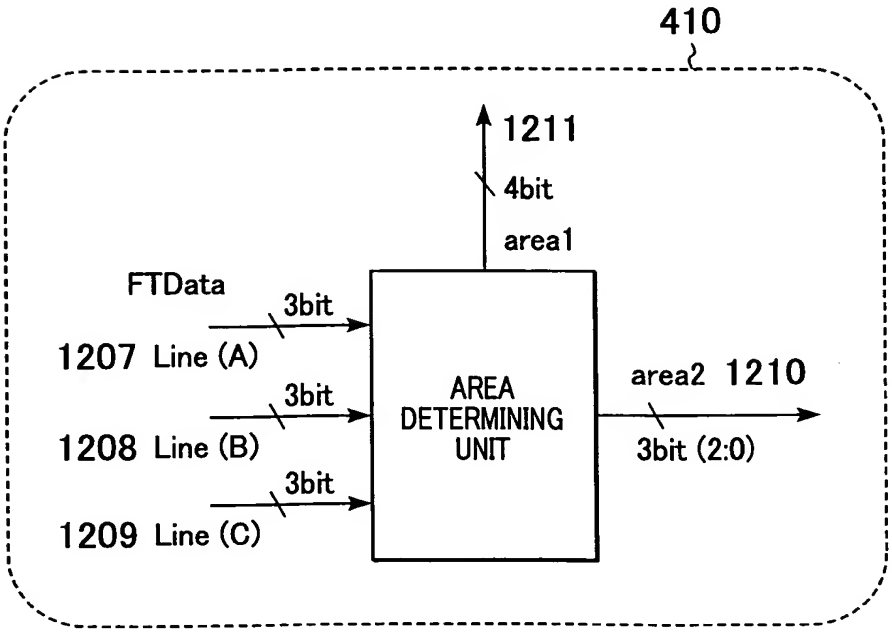


FIG. 13A

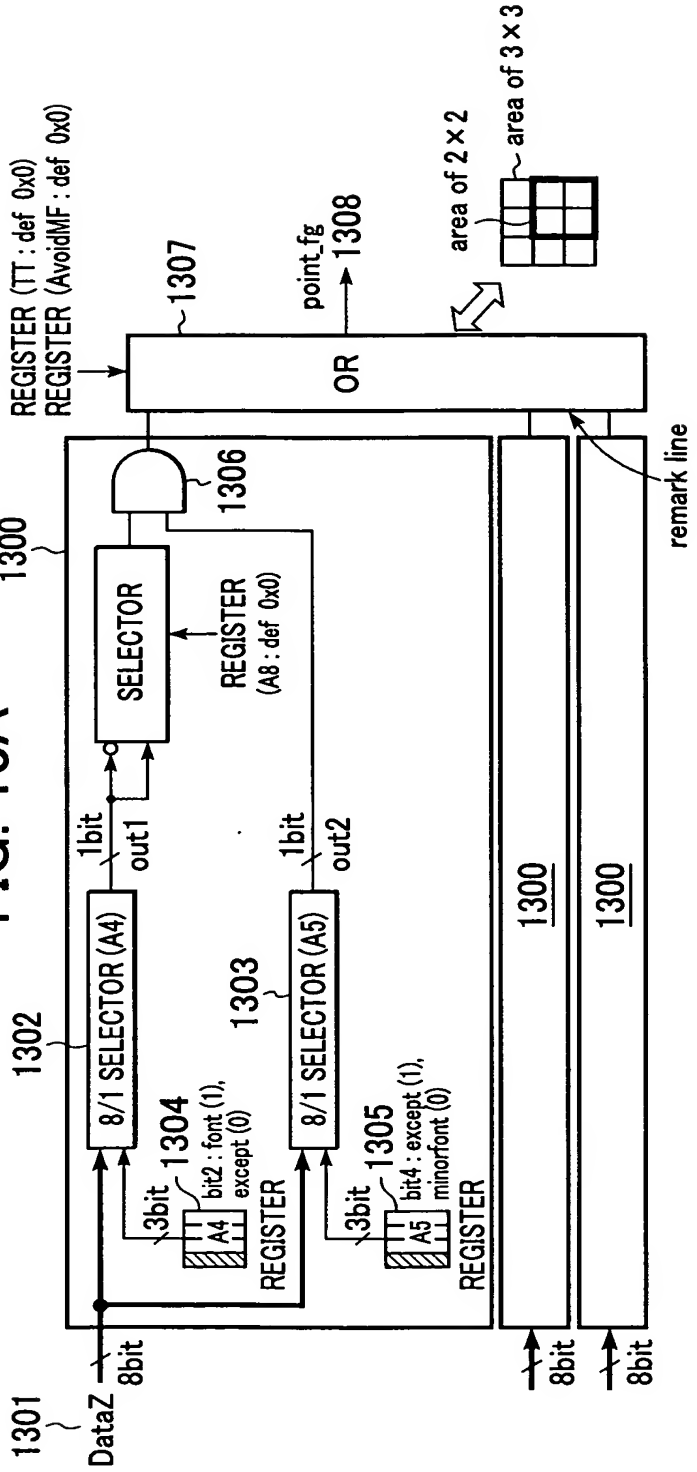


FIG. 13B

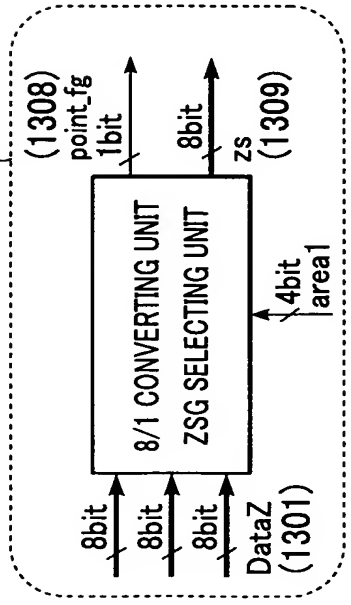


FIG. 13C

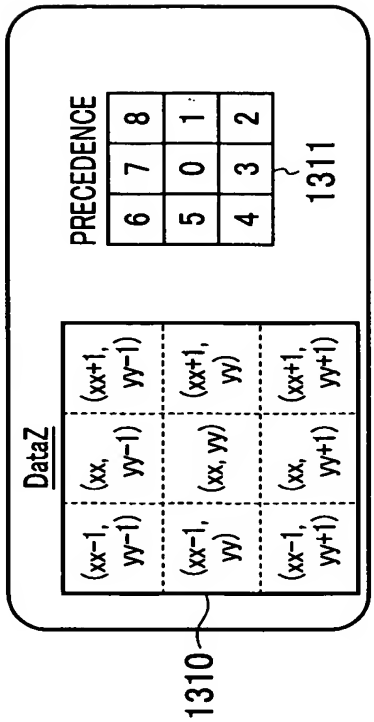


FIG. 14A

1401	1402	1403	1404	1405	1406		
bit3	bit2	bit1	bit0	Table Set			
minor font/line	image	graphic	font/graphic/image	input	output		
0	0	0	0	0	2	No. 2	non (1407)
0	0	0	1	1	3	No. 3~7	font (1408)
0	0	1	0	2	1	No. 1	graphic (1409)
0	0	1	1	3	3	No. 3~7	font/graphic (1410)
0	1	0	0	4	3	No. 3~7	image (1411)
0	1	0	1	5	3	No. 3~7	font/image (1412)
0	1	1	0	6	3	No. 3~7	graphic/image (1413)
0	1	1	1	7	3	No. 3~7	font/graphic/image (1414)
1	0	0	0	8	2	No. 2	non (1415)
1	0	0	1	9	2	No. 2	minor font (1416)
1	0	1	0	10	2	No. 2	minor graphic (1417)
1	0	1	1	11	2	No. 2	minor font/graphic (1418)
1	1	0	0	12	2	No. 2	minor image (1419)
1	1	0	1	13	2	No. 2	minor font/image (1420)
1	1	1	0	14	2	No. 2	minor graphic/image (1421)
1	1	1	1	15	2	No. 2	minor font/graphic (1422)

FIG. 14B

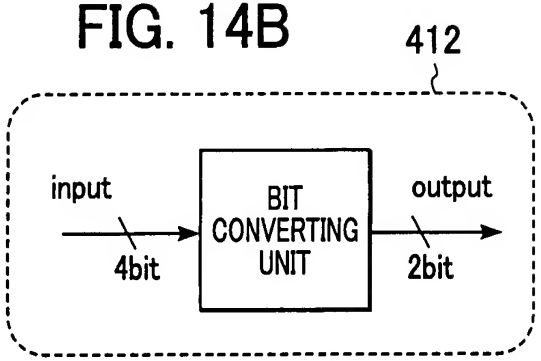


FIG. 15

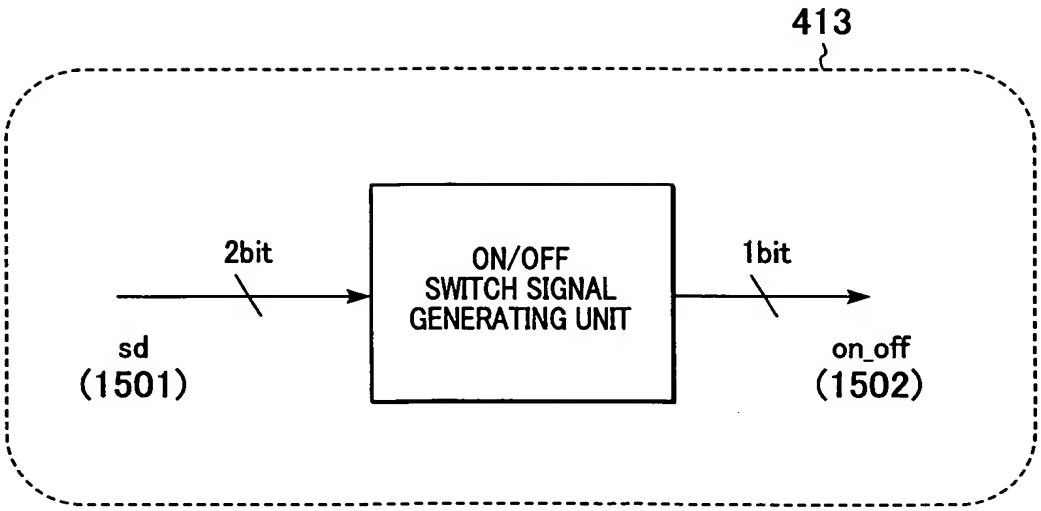

413
2bit
ON/OFF
SWITCH SIGNAL
GENERATING UNIT
1bit
sd
(1501)
on_off
(1502)

FIG. 16A

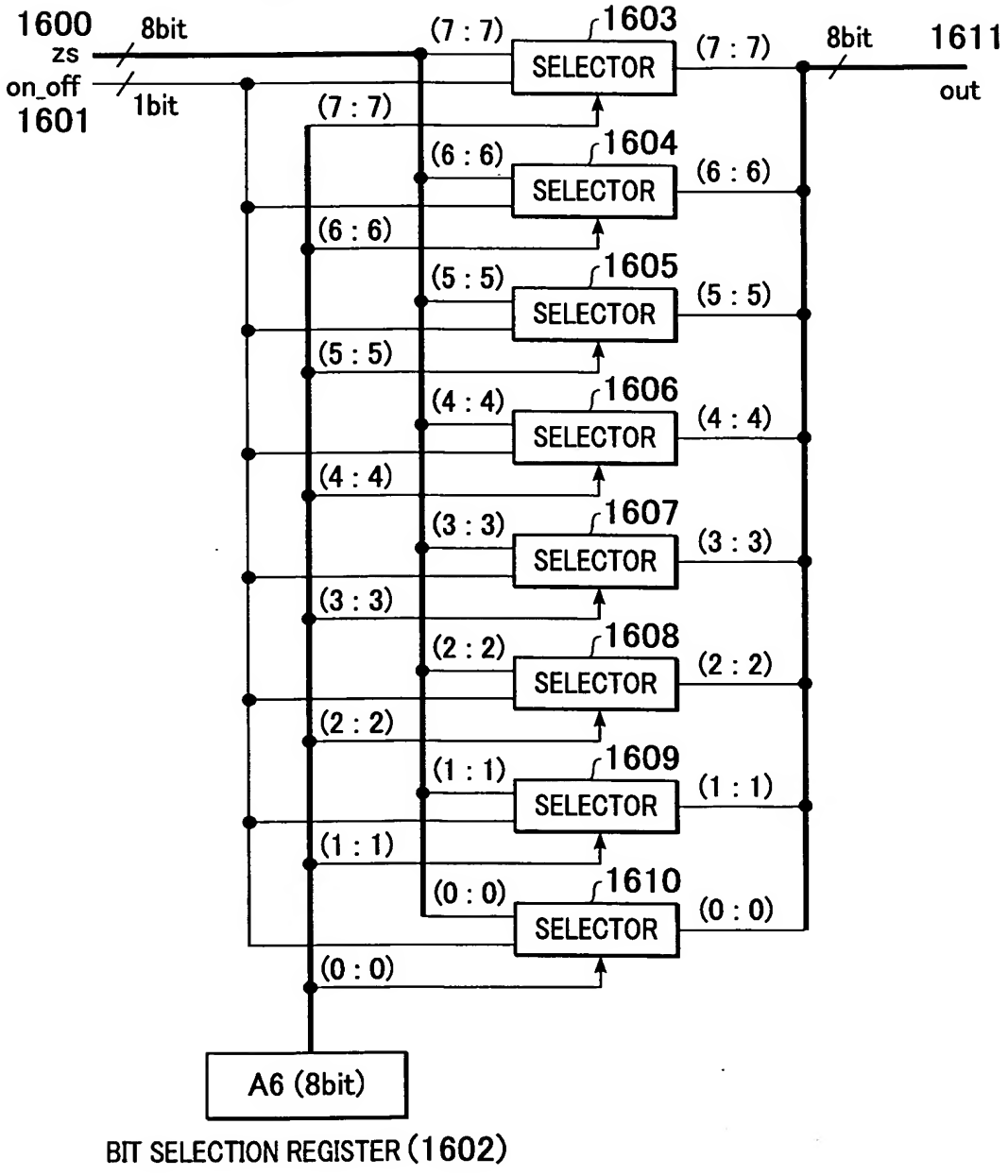


FIG. 16B

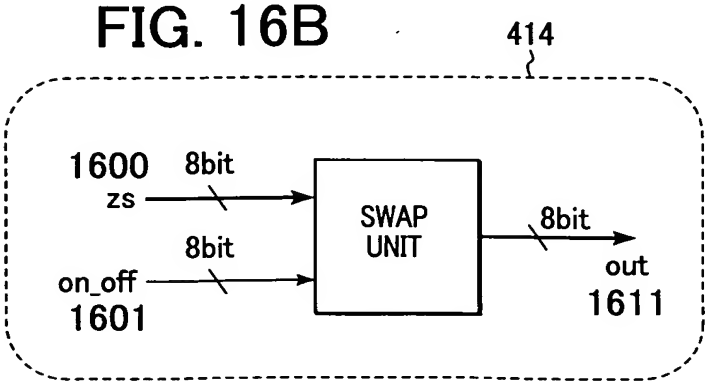


FIG. 17

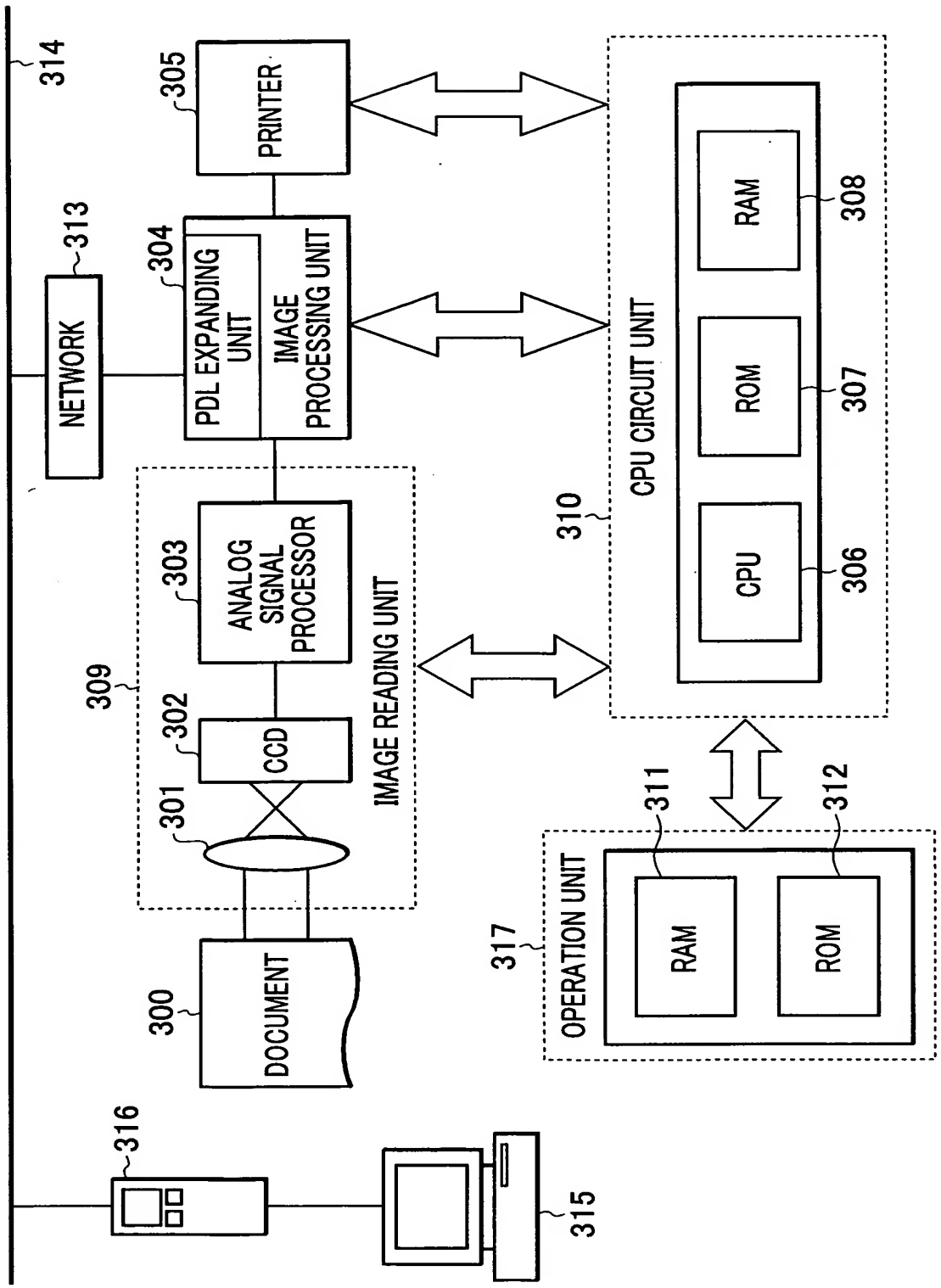

314
305
PRINTER
313
NETWORK
304
PDL EXPANDING UNIT
IMAGE PROCESSING UNIT
CPU CIRCUIT UNIT
RAM
308
ROM
307
CPU
306
310
303
ANALOG SIGNAL PROCESSOR
309
302
CCD
301
IMAGE READING UNIT
311
312
OPERATION UNIT
RAM
ROM
317
300
DOCUMENT
316
315

FIG. 18

no3

7	7	7
7	8	7
7	7	7

no4

6	6	6
6	16	6
6	6	6

no5

4	4	4
4	32	4
4	4	4

no6

2	2	2
2	48	2
2	2	2

no7

1	1	1
1	56	1
1	1	1